

# METHOD AND APPARATUS FOR DRIVING LIQUID CRYSTAL DISPLAY

## BACKGROUND OF THE INVENTION

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### Field of the Invention

This invention relates to a liquid crystal display, and more particularly to a method and apparatus for driving a liquid  
10 crystal display wherein a picture quality can be clearly kept upon conversion of a resolution mode of the liquid crystal display.

### Description of the Related Art

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Generally, a liquid crystal display (LCD) of active matrix driving system uses thin film transistors (TFT's) as switching devices to display a natural moving picture. Since such a LCD can be made into a smaller device in size than the existent Brown  
20 tube, it has been widely used for a computer monitor well as office automation equipment such as a copy machine, etc. and portable equipment such as a cellular phone and a pager, etc.

Such a LCD trends toward a high resolution and a large-scale  
25 screen. Recently, a liquid crystal monitor of a personal computer has supported resolutions required for high-class equipment such as a workstation. Fig. 1 schematically shows such a LCD.

Referring to Fig. 1, the LCD includes a liquid crystal display  
30 panel 2 having TFT's and liquid crystal cells provided between

gate lines GL1 to GLm and data lines DL1 to DLn, a source drive integrated circuit (IC) 6 for supplying a data to the data lines DL1 to DLn, a gate drive IC for sequentially applying scanning pulses to the gate lines GL1 to GLm, a timing controller 8 for  
5 applying required timing control signals to the source drive IC 6 and the gate drive IC 4, and an interface circuit 12 for supplying a data from a graphic card (not shown) to the timing controller 8.

10 The source drive IC 6 samples and latches red (R), green (G) and blue (B) data in response to a source shift clock (SSC) from the timing controller to convert a timing system of 'dot at a time scanning' into that of 'line at a time scanning'. The data converted into a system of 'line at a time scanning' is  
15 synchronized with the scanning pulses and simultaneously applied to n data lines DL1 to DLn.

Timing control signals applied from the timing controller 8 to the source drive IC 6 include a source start pulse (SSP) for  
20 instructing an initiation of a data sampling or latch in one horizontal synchronization interval, a source output enable signal (SOE) for controlling an output of the source drive IC 6 and a polarity control signal (POL) for inverting the polarity of a data upon frame/line/column inversion driving, etc. besides the  
25 SSC.

The gate drive IC 6 includes a shift register and a level shifter, etc. The gate driver IC 6 sequentially applies scanning pulses having a gate high voltage in response to a gate start pulse  
30 (GSP) from the timing controller 8, to thereby charge a data in

the liquid crystal cells.

Timing control signals applied from the timing controller 8 to the gate drive IC 4 include a gate shift clock GSC for determining a time when the gate of the TFT is turned on or off and a gate output enable signal (GOE) for controlling an output of the gate drive IC 4, etc. besides the GSP.

The timing controller 8 receives RGB signals inputted via the interface circuit 12 to distribute it into the source drive IC 6 and control the source drive IC 6 and the gate drive IC 4. The timing controller 8 generates the timing control signals required for the source drive IC 6 and the gate drive IC 4 using the SSC applied from a reference clock generator (not shown).

The interface circuit 12 applies RGB data, a data enable signal I\_DE and a dot clock Dclk from the graphic card (not shown) to the timing controller 8.

The timing controller 8 and the interface circuit 12 may include a LVDS circuit so that they can reduce the number of data supply lines and an electro-magnetic interference.

The VESA (Video Electronics Standard Association) has defined the number of dot clocks Dclk having a frequency of 65Mhz at a blanking interval (or a low logic interval) of a data enable signal I\_DE inputted from the graphic card to the timing controller 8 in resolution modes of UXGA, SXGA, XGA, SVGA and VGA by an even number. However, if the resolution mode is converted from UXGA, SXGA or XGA into SVGA or VGA, the number of dot clocks

Dclk is changed into an odd number. When the resolution mode is converted, a horizontal noise emerges on the screen.

As can be seen from Fig. 2, the conventional timing controller 8 toggles a dot clock Dclk from the interface circuit 12 irrespectively of a resolution conversion of the graphic card to generate the SSC. More specifically, the conventional timing controller 8 operates a reset circuit at a dot clock Dclk generated at the third sequence from a time when the data enable signal I\_DE is changed into a high level independently of a resolution to reset a source shift clock SSC. Herein, as shown in Fig. 3, if a resolution mode is UXGA, SXGA or XGA, the number of dot clocks Dclk (65Mhz in the XGA mode) at a blanking interval of the data enable signal I\_DE is an even number (n). In this case, the source shift clock SSC has normal waveform and frequency. On the other hand, as shown in Fig. 4, if a resolution mode is SVGA or VGA, the number of dot clocks Dclk at a blanking interval of the data enable signal DE is changed into an odd number. As a result, when the resolution mode is converted from UXGA, SXGA or XGA into SVGA or VGA, the source start pulse SSP and the source shift clock SSC inputted to the source shift clock SSC go beyond a timing specification stipulating a set-up time and a hold time to cause a horizontal noise on the screen, as shown in Fig. 5.

In Fig. 3 to Fig. 5, the data enable signal DE is created by an internal circuit of the timing controller 8 to instruct a sampling initiation time of an odd data and an even data divided from an input data by means of the timing controller 8. This can be more easily understood from waveform diagrams of Fig. 9A to Fig. 11B capturing a scope screen. In the waveform diagrams of

Figs. 9A to 11B, the horizontal axis represents a time (i.e., 25.0ns unit), and the vertical axis does a voltage (i.e., 2.0V unit).

5 As can be seen from Fig. 9A and Fig. 9B that represent waveforms of a source start pulse SSP and a source shift clock SSC at the set-up time and the hold time in a resolution of XGA, since the number of dot clocks Dclk in a resolution of XGA is an even number, waveforms of the source start pulse SSP and the source  
10 shift clock SSC take a normal shape. On the other hand, as can be seen from Fig. 10A and Fig. 10B that represent waveforms of the source start pulse SSP and the source shift clock SSC at the set-up time and the hold time when a resolution is converted from XGA into VGA, since the number of dot clocks Dclk is changed from an  
15 even number into an odd number, a period of the source shift clock SSC is changed to distort a waveform of the source shift clock SSC at a conversion time of resolution. Fig. 11A and Fig. 11B shows an overlapped state of waveforms of the source start pulse SSP and the source shift clock SSC at a time when an XGA  
20 resolution is sustained and at a time when a resolution mode is converted from XGA into VGA, respectively.

#### SUMMARY OF THE INVENTION

25 Accordingly, it is an object of the present invention to provide a method and apparatus for driving a liquid crystal display wherein a picture quality can be clearly kept upon conversion of a resolution mode of the liquid crystal display.

30 In order to achieve these and other objects of the invention, a

method of driving a liquid crystal display according to one aspect of the present invention includes the steps of receiving a data enable signal for indicating a time interval when a video data exists; detecting an enable initiation time of the data enable signal; generating a reset signal at said enable initiation time of the data enable signal; and resetting a source shift clock for sampling the video data in response to the reset signal.

The method further includes the steps of sampling and then latching the video data in response to the source shift clock; applying the latched video data to data lines of a liquid crystal display panel; and sequentially applying scanning pulses to gate lines of the liquid crystal display panel.

A driving apparatus for a liquid crystal display according to another aspect of the present invention includes a source shift clock reset unit for detecting an enable initiation time of a data enable signal for indicating a time interval when a video data exists to generate a reset signal; and a reference clock generator for generating a source shift clock for sampling the video data at said enable initiation time, wherein the source shift clock is reset at said enable initiation time in response to the reset signal.

The driving apparatus further includes a liquid crystal display panel having liquid crystal cells provided at pixel areas between the data lines and the gate lines perpendicularly crossing each other and thin film transistors provided at intersections between the data lines and the gate lines to drive the liquid crystal

cells; a source driver for sampling and then latching the video data in response to the source shift clock and for applying the latched data to the data lines of the liquid crystal display panel; and a gate driver for sequentially applying scanning pulses to the gate lines of the liquid crystal display panel to select scanning lines; and a timing controller for controlling the source driver and the gate driver.

In the driving apparatus, the source shift clock reset unit and the reference clock generator are included in the timing controller.

The source shift clock reset unit includes a D flip-flop for receiving the data enable signal and a dot clock via an input line to delay the data enable signal in accordance with the dot clock; an inverter for inverting the delayed data enable signal; and an AND gate for making a logical product operation of the delayed and inverted enable signal and the data enable signal from the input line to generate a high logic signal for indicating an enable initiation time of the data enable signal; and a reset part for generating a reset signal for resetting the source shift clock in response to the high logic signal generated in the AND gate.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings, in

which:

Fig. 1 is a schematic block diagram showing a configuration of a driving apparatus for a conventional liquid crystal display;

Fig. 2 is an output waveform diagram of the timing controller shown in Fig. 1;

Fig. 3 is an input/output waveform diagram of the timing controller shown in Fig. 1 in the resolution modes of UXGA, SXGA and XGA;

Fig. 4 is an input/output waveform diagram of the timing controller shown in Fig. 1 in the resolution modes of VGA and SVGA;

Fig. 5 is an input/output waveform diagram of the timing controller shown in Fig. 1 in the resolution modes of XGA and VGA;

Fig. 6 is a schematic block diagram showing a configuration of a driving apparatus for a liquid crystal display according to an embodiment of the present invention;

Fig. 7 is a detailed circuit diagram of the source shift clock reset unit shown in Fig. 6;

Fig. 8 is an input/output waveform diagram of the driving apparatus for the liquid crystal display according to the embodiment of the present invention;

Fig. 9A is a waveform diagram of a source start pulse and a source shift clock appearing at a set-up time in a resolution of XGA;

Fig. 9B is a waveform diagram of a source start pulse and a source shift clock appearing at a hold time in a resolution of XGA;

Fig. 10A is a waveform diagram of a source start pulse and a source shift clock appearing at a set-up time in a resolution of



VGA;

Fig. 10B is a waveform diagram of a source start pulse and a source shift clock appearing at a hold time in a resolution of VGA;

5 Fig. 11A depicts an overlapped state of the waveforms in Fig. 9A and Fig. 10A; and

Fig. 11B depicts an overlapped state of the waveforms in Fig. 9B and Fig. 10B.

## 10 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Fig. 6, there is shown a driving apparatus for a liquid crystal display (LCD) according to an embodiment of the present invention.

15 The LCD includes a liquid crystal display panel 62 having TFT's and liquid crystal cells provided between gate lines GL1 to GLm and data lines DL1 to DLn, a source drive integrated circuit (IC) 66 for supplying a data to the data lines DL1 to DLn, a gate  
20 drive IC 64 for sequentially applying scanning pulses to the gate lines GL1 to GLm, a timing controller 68 for applying required timing control signals to the source drive IC 66 and the gate drive IC 64, a source shift clock (SSC) generator 60 for  
25 receiving a dot clock Dclk and a data enable signal I\_DE to generate a source shift clock SSC, and an interface circuit 72 for supplying a data from a graphic card (not shown) to the timing controller 72.

The source drive IC 66 samples and latches red (R), green (G) and  
30 blue (B) data in response to a source shift clock SSC from the

SSC generator 60 and thereafter applies a data to n data lines DL1 to DLn simultaneously in synchronization with scanning pulses.

The gate drive IC 64 includes a shift register and a level shifter, etc. The gate driver IC 64 sequentially applies scanning pulses having a gate high voltage in response to a gate start pulse (GSP) from the timing controller 68.

The timing controller 68 receives RGB signals inputted via the interface circuit 72 to distribute them into the source drive IC 66 and generates timing control signals to control the source drive IC 66 and the gate drive IC 64.

The interface circuit 72 applies RGB data, a data enable signal I\_DE and a dot clock Dclk from the graphic card (not shown) to the timing controller 68.

The SSC generator 60 includes a source shift clock (SSC) reset unit 60a and a reference clock generator 60b. The SSC reset unit 60a receives a dot clock Dclk and a data enable signal I\_DE. The SSC reset unit 60a senses a time when a data enable signal I\_DE is changed into a high level irrespectively of the number of dot clocks Dclk upon conversion of a resolution mode to generate a reset signal (RESET) at the time when a data enable signal I\_DE is changed into a high level and supplies the reset signal (RESET) to the reference clock generator 30. The reference clock generator 30 generates a source shift clock and resets the source shift clock (SSC) at the time when a data enable signal I\_DE is changed from a low logic into a high logic in response to the reset signal (RESET). The reference clock generator 30 applies

the source shift clock SSC to the source drive IC 6. The SSC generator 60 may be included in the timing controller 68.

As shown in Fig. 7, the SSC reset unit 60a includes a D flip-flop 21 receiving the data enable signal I\_DE and the dot clock Dclk from the interface circuit 72, an inverter 23 connected to an output terminal of the D flip-flop 21, a buffer 22 receiving a data enable signal I\_DE via an I\_DE input line 26, an AND gate commonly connected to output terminals of the buffer 22 and the inverter 23, and a reset part 25 connected between a Dclk input line 27 and the output terminal of the AND gate 24.

The D flip-flop 21 outputs a data enable signal I\_DE whenever the dot clock Dclk is inputted, to thereby delay the data enable signal I\_DE by one period of the dot clock Dclk. Herein, a frequency of the dot clock Dclk is assumed to be 65Mhz.

The buffer 22 applies a data enable signal I\_DE inputted via the I\_DE input line 26 to a first input terminal of the AND gate 24, and the inverter 23 inverts the data enable signal I\_DE delayed by the D flip-flop 21 and applies it to a second input terminal of the AND gate 24.

The AND gate 24 makes a logical product operation of the data enable signal I\_DE from the buffer 22 and the delayed and inverted data enable signal I\_DE from the inverter to generate a signal indicating a time when the data enable signal I\_DE is changed from a low logic into a high logic.

The reset part 25 generates a reset signal (RESET) for resetting

the source shift clock SSC in response to a high logic signal inputted from the AND gate 24 and supplies the reset signal (RESET) to the reference clock generator.

Referring to Fig. 8, the dot clock Dclk of 65Mhz is commonly  
5 inputted to the D flip-flop 21 and the reset part 25 to synchronize a signal outputted from the AND gate 24 with a signal outputted from the reset part 25. If the data enable signal I\_DE is at a blanking interval that is, has a low logic, then an output signal of the AND gate 24 remains at a low logic because  
10 an output signal of the buffer 22 maintains a low logic. Since output signals of the buffer 22 and the inverter 23 have a high logic simultaneously at a time when the data enable signal I\_DE is changed from a low logic into a high logic, the AND gate 24 generates a high logic of pulse signal. In other words, the AND  
15 gate 24 detects a time when a logic value of the data enable signal I\_DE is changed from a low logic into a high logic irrespectively of a change in the number of dot clocks upon conversion of a resolution mode, for example, upon conversion from UXGA, SXGA or XGA into SVGA or VGA. The pulse signal  
20 generated from the AND gate 24 in this manner is applied to the reset part 25 to reset a source shift clock (SSC) of 32.5Mhz outputted from the reference clock generator 30. Accordingly, the source shift clock SSC inputted to the source drive IC 66 always has a normal pulse width and frequency in an enable interval of  
25 the data enable signal I\_DE independently of a conversion of resolution mode.

The source start pulse SSP is generated at twice pulse width the source shift clock SSC between the odd and even data and the  
30 reset signal by means of the timing controller 68.

As described above, according to the present invention, an initiation time of an enabling interval of the data enable signal I\_DE inputted to the timing controller is detected irrespectively  
5 of an odd/even change of the dot clock Dclk caused by a resolution conversion to reset the source shift clock SSC. As a result, the source shift clock SSC and the source start pulse SSP inputted to the source drive IC meets a timing specification in the VESA standard independently of an odd/even change of the dot  
10 clock Dclk upon conversion of a resolution mode, for example, upon conversion from UXGA, SXGA or XGA mode into SVGA or VGA mode, so that it becomes possible to prevent a generation of horizontal noise upon conversion of a resolution mode. Furthermore, according to the present invention, timing margins of the source  
15 shift clock SSC and the source start pulse SSP inputted to the source drive IC are assured, so that it becomes possible to keep a clear picture under a low temperature or high temperature environment.

20 Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without  
25 departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.